## IN THE UNITED STATES DISTRICT COURT FOR THE EASTERN DISTRICT OF TEXAS MARSHALL DIVISION

OPTi Inc.			)	
	v.	Plaintiff,	)	Civil Action No. 2:07CV021(TJW)
	٧.		)	CIVII / CHOII 1 (0. 2.0/ C V 021 (13 W)
Apple, Inc.			)	
			)	
		Defendant.	)	

## **CLAIM CONSTRUCTION ORDER**

This case came before the Court on November 26, 2008 for hearing on all claim construction issues pursuant to the Docket Control Order in this matter. The Court has reviewed the briefs of the parties and the argument had in open Court. Having carefully considered the parties arguments, the language of the claims in light of the specification and the pertinent portions of the prosecution history, and having evaluated the disputed claim terms in light of the principles of claim announced by the Federal Circuit, particularly as set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*), the Court rules as set forth below as to the claim terms in dispute between the parties and enters as its order the claim constructions agreed to by the parties.

<b>U.S. Patent 5,710,906</b>	Term/Element for	Court's	Agreed
Claim 9	Construction	Construction	Construction
[9.1] A method for	"first cache	[AGREED]	the first level of
transferring data between a	memory"		cache memory,
bus master and a plurality of			commonly referred
memory locations at			to as L1 cache
respective addresses in an			memory.
address space of a secondary	"said first cache	[AGREED]	See "first cache
memory, for use with a host	memory"		memory"
processing unit and a first	"secondary	[AGREED]	memory located

U.S. Patent 5,710,906	Term/Element for	Court's	Agreed
Claim 9	Construction	Construction	Construction
cache memory which caches memory locations of said secondary memory for said host processing unit, said first cache memory having a line size of L bytes, comprising the steps of:	memory"		logically behind the first level cache memory, i.e., DRAM memory and, if present, L2 and L3 cache memory.
	"bus master"	[AGREED]	An I/O-bus device that initiates a data transfer on an I/O bus
[9.2] sequentially transferring at least three data units between said bus master and said secondary memory beginning at a first starting memory location address in said secondary memory address space and continuing sequentially beyond an L-byte boundary of said secondary	"sequentially transferring at least three data units between said bus master and said secondary memory"  "said bus master"	[AGREED]	moving at least three data units between the bus master and the secondary memory in the sequence in which they are stored.  See Limitation 9.1.
memory address space; and [9.3] prior to completion of the transfer of the first data unit beyond said L-byte boundary, determining whether an N+1'th L-byte line of said secondary memory is	"prior to the completion of the transfer of the first data unit beyond said L-byte boundary"	[AGREED]	prior to completion of the transfer of the first data unit beyond said L-byte boundary.
cached in a modified state in said first cache memory, said N+1'th L-byte line being the line of said secondary memory which includes said first data unit beyond said L-byte boundary,	"determining whether an N+1'th L-byte line of said secondary memory is cached in a modified state in said first cache memory"	[AGREED]	determining whether the N+1th line of data in the first cache memory is different from the corresponding data in secondary memory
[9.4] all of said transfers of data units in said step of sequentially transferring, occurring at a constant rate.	"said transfers of data units in said step of sequentially transferring"	[AGREED]	See Limitation 9.2 "sequentially transferring at least three data units between said bus master and said secondary memory."

U.S. Patent 5,710,906	Term/Element for	Court's	Agreed
Claim 9	Construction	Construction	Construction
	"constant rate"	[AGREED]	A uniform rate
	"all of said	[AGREED]	Each and every
	transfers of data		one of the at least
	units"		three transfers of
			data units

U.S. Patent No. 6,405,291 Claim 73	Term/Element for Construction	Court's Construction	Agreed Construction
[73.1] A method for transferring a plurality of data	"secondary memory"	[AGREED]	See '906 Patent, Limitation 9.1
units to a bus master from a	memory		Lillitation 9.1
respective plurality of memory locations at			
1			
sequential memory location addresses in an address space			
of a secondary memory, for		5.4.65.777.3	G (00.17)
use with a host processing	"bus master"	[AGREED]	See '906 Patent,
unit and a cache memory			Limitation 9.1
which caches memory			
locations of said secondary			
memory for said host			
processing unit, said cache			
memory having a line size of			
L bytes, and each data unit	"said bus master"	[AGREED]	See '906 Patent,
having a size equal to the			Limitation 9.1
largest size that can be			
transferred to said bus master			
in parallel, comprising the			
steps of:			
[73.2] sequentially	"sequentially	[AGREED]	moving data units
transferring data units to said	transferring data	[101022]	to the bus master
bus master from said	units to said bus		from the secondary
secondary memory according	master from said		memory in the
to a PCI-bus burst transaction,	secondary		sequence in which
beginning at a starting	memory"		they are stored
memory location address in			
said secondary memory			
address space and continuing			
beyond at least first and			
second L-byte boundaries of	"said bus master"	[AGREED]	See '906 Patent,
said secondary memory			Limitation 1.1

U.S. Patent No. 6,405,291	Term/Element for	Court's	Agreed
Claim 73	Construction	Construction	Construction
address space, each L-byte line of said transaction			
requiring at least 8 data unit			
transfers to said bus master;			
and			
[73.3] during the transfer of the data units for each entire	"during the transfer of the	[AGREED]	while the data units for each
N'th L-byte line in said step	data units for each		entire N'th L-byte
of transferring, initiating one	entire N'th L-byte		line are moving to
and only one snoop access of	line"		the bus master
said cache memory, said			from the secondary
snoop accesses each			memory
specifying the respective	"the transfer of	[AGREED]	See Limitation
N+1'th L-byte line and being	the data units"		73.2 "sequentially
initiated early enough such that they can be sampled by			transferring data units to said bus
said host processing unit prior			master from said
to completion of the transfer			secondary
to said bus master of the last			memory."
data unit in the respective	"N+1'th L-byte	[AGREED]	the next sequential
N'th L-byte line,	line"		line following line N
	"initiating one and	initiating one and	
	only one snoop	only one next-line	
	access of said	inquiry of said	
	cache memory"	cache memory	
	"snoop access"	Next-line inquiry	
F70 41 1 1 1 1 2	(/ • • • • • •	LA CREED?	
[73.4] wherein said step of	"said step of	[AGREED]	See Limitation
transferring comprises the step of transferring to said bus	transferring"		73.2 "sequentially transferring data
master three sequential data			units to said bus
units including the last data			master from said
unit before said first L-byte			secondary
boundary and the first data			memory."
unit beyond said first L-byte	"constant rate"	[AGREED]	A uniform rate
line, all at a <b>constant rate</b> ,	"coid stop of	[VCDEED]	See Limitation
[73.5] and wherein said step of transferring further	"said step of transferring"	[AGREED]	73.2 "sequentially
comprises the step of	ci ansici i ing		transferring data

U.S. Patent No. 6,405,291	Term/Element for	Court's	Agreed
Claim 73	Construction	Construction	Construction
transferring to said bus master			units to said bus
three sequential data units			master from said
including the last data unit			secondary
before said second L-byte			memory."
boundary and the first data			
unit beyond said second L-			
byte line, all at a constant rate.			

U.S. Patent No. 6,405,291	Term/Element for	Court's	Agreed
Claim 74	Construction	Construction	Construction
[74.1] A method according to	"said step of	[AGREED]	See Limitation
claim 73, wherein said step of	sequentially		73.2 "sequentially
sequentially transferring data	transferring data		transferring data
units continues further beyond	units"		units to said bus
a third L-byte boundary of			master from said
said secondary memory, and			secondary
wherein said step of			memory."
transferring further comprises	"said step of	[AGREED]	See Limitation
the step of transferring three	transferring"		73.2 "sequentially
sequential data units including			transferring data
the last data unit before said			units to said bus
third L-byte boundary and the			master from said
first data unit beyond said			secondary
third L-byte line, all at a			memory."
constant rate.	"constant rate"	[AGREED]	See Limitation
			73.4

U.S. Patent No. 6,405,291	Term/Element for	Court's	Agreed
Claim 88	Construction	Construction	Construction
[88.1] Controller apparatus for a	"cache memory"	[AGREED]	See Limitation
computer system which	0.000.00 1.101.101.01.01	[]	73.1
includes a secondary memory			
having an address space, a bus			
master, a host processing unit	"secondary	[AGREED]	See '906 Patent,
and a cache memory which	memory"	[TOTELLE]	Limitation 9.1
caches memory locations of			2
said secondary memory for said			
host processing unit, said cache	"said cache	[AGREED]	See Limitation
memory having a line size of L	memory"		73.1
bytes, and each data unit having	, and the second		
a size equal to the largest size			
that can be transferred to said	(6baa-t-a22	[ACDEED]	Car (OOC Datant
bus master in parallel, said	"bus master"	[AGREED]	See '906 Patent, Limitation 9.1.
controller apparatus comprising			Lillitation 9.1.
circuitry which in a mode of	"said bus master"	[AGREED]	See '906 Patent,
operation, in response to a PCI-	said bus master	[AGKEED]	Limitation 9.1.
bus burst read transaction			Lillitation 9.1.
initiated by said bus master,			
[88.2] sequentially transfers	"sequentially	[AGREED]	moving data units
data units to said bus master	transfers data units		to the bus master
from said secondary memory	to said bus master		from the secondary
according to said PCI-bus burst	from said secondary		memory in the
transaction, beginning at a	memory"		sequence in which
starting memory location	((	[A CDEED]	they are stored
address in said secondary	"constant rate"	[AGREED]	See '906 Patent,
memory address space and continuing beyond at least first,		[ACDEED]	Limitation 9.4
second and third L-byte	"at a constant rate"	[AGREED]	See '906 Patent,
boundaries of said secondary	"a a a a a a a a a a a a a a a a a a a	[ACDEED]	Limitation 9.4
memory address space, each full	"sequentially	[AGREED]	This is not a
L-byte line of said transaction	transfers data units to said bus master		This is not a
requiring at least 8 data unit			means-plus- function element
transfers to said bus master, a	from said secondary memory according		and, therefore, it
plurality of sequential data units	to said PCI-bus		need not be
bracketing at least said first,	burst transaction,		construed
second and third L-byte	beginning at a		according to 35
boundaries being transferred to	starting memory		U.S.C. §112 ¶ 6.
said bus master at a constant	location address in		0.b.c. 5112    0.
rate, said constant rate being	said secondary		
dependent upon the frequency	memory address		
of a PCI-bus clock provided to	space and		
said bus master; and	continuing beyond		
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U.S. Patent No. 6,405,291	Term/Element for	Court's	Agreed
Claim 88	Construction	Construction	Construction
	at least first, second		
	and third L-byte		
	boundaries of said		
	secondary memory		
	address space, each		
	full L-byte line of		
	said transaction		
	requiring at least 8		
	data unit transfers		
	to said bus master, a		
	plurality of		
	sequential data units		
	bracketing at least		
	said first, second		
	and third L-byte		
	boundaries being		
	transferred to said		
	bus master at a		
	constant rate, said		
	constant rate being		
	dependent upon the		
	frequency of a PCI-		
	bus clock provided		
	to said bus master"		

SIGNED this 4th day of December, 2008.

CHARLES EVERINGHAM IV

UNITED STATES MAGISTRATE JUDGE